AMENDMENTS TO THE CLAIMS

Claims 1-13. (Previously canceled).

Claim 14. (Previously amended). A method of manufacturing a semiconductor device according to claim 23, further comprising:

forming a passivation film on the third interlayer insulating film, the passivation film exposing the bonding pad.

Claim 15. (Previously amended). A method of manufacturing a semi conductor device according to claim 14, wherein the passivation film is formed by forming a silicon oxide film and a silicon nitride film.

Claim 16. (Previously amended). A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

Claim 17. (Original). A method of manufacturing a semiconductor device according to claim 16, further comprising a step of planarizing the second silicon oxide film by CMP.

Claim 18. (Original). A method of manufacturing a semiconductor device according to claim 16, further comprising a step of planarizing the second silicon oxide film by etching.

Claim 19. (Previously amended). A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) comprises of:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film of the base layer;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers.

Claim 20. (Previously amended). A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) comprises:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film by sputtering:

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layers.

Claim 21. (Previously amended). A method of manufacturing a semiconductor device according to claim 23, wherein the step (c) comprises:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers by plasma CVD.

Claim 22. (Previously amended). A method of manufacturing a semiconductor device according to claim 23, wherein the step (b) of forming the first conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

Claim 23. (Currently amended). A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) simultaneously forming a first conductive pad and a first wiring layer on the insulating film;

(c) forming a first interlayer insulating film on [both] the first conductive pad, the first wiring layer and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film, each of the first through holes extending from the first conductive pad or the first wiring layer respectively, to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) simultaneously forming a second conductive pad and a second wiring layer on the first interlayer insulating film, each of the second conductive pad and the second wiring layer being in contact with the conductive material in one or more of the plurality of first through holes;

(g) forming a second interlayer insulating film on the second conductive pad, the second wiring layer and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film, each of the ~~first~~ second through holes extending from the second conductive pad or the second wiring layer, respectively, to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) simultaneously forming a third conductive pad and a third wring layer on the second interlayer insulating film, each of the third conductive pad and wiring layer being in contact with the conductive material in one or more of the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on ~~both~~ the third conductive pad, the third wiring layer and the second interlayer insulating film;

(l-1) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive ~~pad, the through hole being formed so that at least two side wall laminations abutting the third interlayer insulating film are located around edges of the through hole; and~~ pad;

(l-2) forming a conductive portion covering a side wall of the through hole through the third interlayer insulating film so that part of the third conductive pad is exposed; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

Claim 24. (Presently amended). A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film;

(2) forming a base layer insulating film on the conductive pad, the wiring layer and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film, each of the through base holes extending from the conductive pad or the wiring layer, respectively, to an upper surface of the base layer insulating film;

(4) filling the base through holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each

of the respective intermediate layers being formed by carrying out at least the following steps:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film of the immediately preceding layer, each of the conductive pad and wiring layer being in contact with the conductive material in one or more of the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on the conductive pad, the wiring layer and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, each of the through holes extending from the conductive pad or wiring layer, respectively, of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in that plurality of through holes in the insulating film of the nth intermediate layer which are in contact with the conductive pad of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3-a) forming an upper through hole through the upper layer insulating film, ~~said~~ the upper through hole being substantially the same size as the conductive pad of the upper ~~layer, the upper through hole being formed so that at least two side wall lamination abutting the upper layer insulating film are located around edges of the through hole; and~~ layer;

(3-b) forming a conductive portion covering a side wall of the upper through hole so that part of the conductive pad of the upper layer is exposed; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

Claim 25. (Previously amended). A method of manufacturing a semiconductor device according to claim 24, further comprising:

(e) forming a passivation film on the upper layer insulating film, the passivation film exposing the bonding pad.

Claim 26. (Previously presented). A method of manufacturing a semiconductor device according to claim 25, wherein the passivation film is formed by forming a silicon oxide film and a silicon nitride film.

Claim 27. (Previously amended). A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

Claim 28. (Previously amended). A method of manufacturing a semiconductor device according to claim 27, further comprising a step of planarizing the second silicon oxide film by CMP.

Claim 29. (Previously amended). A method of manufacturing a semiconductor device according to claim 27, further comprising a step of planarizing the second silicon oxide film by etching.

Claim 30. (Previously amended). A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layers.

Claim 31. (Previously amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film by sputtering;

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layer.

Claim 32. (Previously amended). A method of manufacturing a semiconductor device according to claim 24, wherein the step (b)(4) comprises:

forming Ti films covering an inner surface of the through holes in the base layer insulating film;

forming TiN layers on the Ti films; and

forming W layers on the TiN layer by blanket CVD.

Claim 33. (Previously amended). A method of manufacturing a semiconductor device according to claim 24, wherein the step (c)(1) of forming the conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

Claim 34. (Currently amended). A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a multi-level sub-structure on an underlying insulating layer which is formed over a semiconductor substrate by repeating the steps of;

(1) forming a conductive layer;

(2) patterning the conductive layer to leave a wiring region and a pad region;

(3) forming an insulating layer over the patterned wiring and pad regions;

(4) forming a wiring via hole through the insulating layer above the wiring region and a plurality of pad via holes through the insulating layer above the pad region;

(5) embedding the via holes with conductive material to form a wiring via connected to ~~said~~ the wiring region and a plurality of pad vias connected to ~~said~~ the pad region;

(b) forming an upper conductive layer on a surface of the multi-level sub-structure;

(c) patterning the upper conductive layer to leave an upper wiring region and an upper pad region;

(d) forming an upper insulating layer over the upper wiring region and the upper pad region;

(e-1) forming an upper wiring via hole through the upper insulating layer above the upper wiring region ~~and~~ so as to form an opening which exposes a central region of the upper pad region encompassing a region above said plurality of pad vias~~,~~ ~~the opening being formed so that at least two side wall laminations abutting the upper insulating layer are located around edges of the opening~~;

(e-2) forming a conductive portion covering a side wall of the upper wiring via hole so that part of the upper pad region is exposed; and

(f) forming an uppermost wiring region connected to said upper wiring region and an uppermost pad region connected to said upper pad region, wherein the wiring regions and the pad regions are respectively vertically registered.

Claim 35. (Previously presented). A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a first conductive pad on the insulating film;

(c) forming a first interlayer insulating film on both the first conductive pad and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) forming a second conductive pad on the first interlayer insulating film [and] in contact with the conductive material in the plurality of first through holes;

(g) forming a second interlayer insulating film on both the second conductive pad and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film extending from the second conductive pad to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) forming a third conductive pad on the second interlayer insulating film and in contact with the conductive material in the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film,

wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the first silicon oxide film;

thermally treating the hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

Claim 36. (Previously presented). A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by CMP.

Claim 37. (Previously presented). A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by etching.

Claim 38. (Previously presented). A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) forming a conductive pad on the insulating film;

(2) forming a base layer insulating film on both the conductive pad and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film which through holes extend from the conductive pad to an upper surface of the base layer insulating film;

(4) filling the base though holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) forming a conductive pad on the insulating film of the immediately preceding layer in contact with the conductive material in the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on both the conductive pad and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, the through holes extending from the conductive pad of the respective

intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in the plurality of through holes in the insulating film of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

Claim 39. (Previously presented). A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by CMP.

Claim 40. (Previously presented). A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by etching.

Claim 41. (Previously presented). A method of manufacturing a semiconductor device according to claim 23, wherein the sidewall lamination include Ti, TiN and W layers.

Claim 42. (Previously presented). A method for manufacturing a semiconductor device according to claim 24, wherein the the sidewall lamination include Ti, TiN and W layers.

Claim 43. (Previously presented). A method of manufacturing a semiconductor device according to claim 34, wherein the sidewall lamination include Ti, TiN and W layers.

Claim 44. (New) . A method of manufacturing a semiconductor device according to claim 23, wherein the conductive portion formed in step (1-2) is formed to cover the entire side wall of the through hole.

Claim 45. (New). A method of manufacturing a semiconductor device according to claim 23, wherein the step (1-2) comprises forming a conductive layer on the third interlayer insulating film and anisotropically etching the conductive layer to leave the conductive portion on the side wall of the through hole.

Claim 46. (New). A method of manufacturing a semiconductive device according to claim 45, wherein the step (1-1) also forms a third through hole through the third interlayer insulating film on the third wiring layer, and the step (1-2) forms a conductive filler in the third through hole.

Claim 47. (New). A method of manufacturing a semiconductor device according to claim 24, wherein the conductive portion formed in step (d)(3-b) is formed to cover the entire side wall of the through hole.

Claim 48. (New). A method of manufacturing a semiconductor device according to claim 24, wherein the step (d)(3-b) comprises forming a conductive layer on the third interlayer insulating film and anisotropically etching the conductive layer to leave the conductive portion on the side wall of the through hole.

Claim 49. (New). A method of manufacturing a semiconductive device according to claim 48, wherein the step (d)(3-a) also forms a third through hole through the third interlayer insulating film on the third wiring layer, and the step (d)(3-b) forms a conductive filler in the third through hole.

Claim 50. (New). A method of manufacturing a semiconductor device according to claim 34, wherein the conductive portion formed in step (e-2) is formed to cover the entire side wall of the through hole.

Claim 51. (New). A method of manufacturing a semiconductor device according to claim 34, wherein the step (e-2) comprises forming a conductive layer on the third interlayer insulating film and anisotropically etching the conductive layer to leave the conductive portion on the side wall of the through hole.

Claim 52. (New). A method of manufacturing a semiconductive device according to claim 51, wherein the step (e-1) also forms a third through hole through the third interlayer insulating film on the third wiring layer, and the step (e-2) forms a conductive filler in the third through hole.